means to which an output signal of said first decoding means and an erasure signal are input; and

a local row decoder for selecting [each] a word line by a global word line signal outputted from said global row decoder.

3. (Amended) The decoder circuit of claim 1, wherein said local row decoder is consisted of [;]:

[a first and second transistors to said word line signal is input;

and a third, fourth and fifth transistors outputting a first voltage supply signal and a second voltage supply signal to a sector word line]

a first switching element for transferring a column sector address to a node according to said global word line signal;

a second switching element for transferring a first signal to said node according to said global word line signal;

a third switching element connected, in parallel, with said first switching element, said third switching element operated by potential of a word line;

a fourth switching element for transferring a first signal to said word line according to potential of said node; and

a fifth switching element for transferring a second signal to said word line according to potential of said node.

4. (Amended) The decoder circuit of claim 3 wherein said second, third and fourth [transistors] switching elements are consisted of PMOS transistor, respectively, said first and fifth [transistors] switching elements are consisted of a NMOS transistor, respectively.

5. (Amended) A decoder circuit in a flash memory device, comprising:

[a global row decoder for outputting a global word line signal; and

a local row decoder for selecting a word line in response to said global word line signal of said global row decoder]

a global row decoder for outputting a global word line signal, wherein said global row decoder comprises:

a first transistor for transferring a first voltage to a node according to a first signal;

a second transistor for transferring a ground voltage to said node according to said first signal;

a third transistor for transferring a second voltage to a global word line according to potential of said node; and

a fourth transistor for transferring said first voltage to said global word line according to potential of said node;

a local row decoder for selecting a word line in response